## ABSTRACT OF THE DISCLOSURE

A digital multilevel bit memory array system comprises regular memory arrays and redundant memory arrays. A regular y-driver corresponds to each memory array to read or write contents to a multilevel bit memory cell and compare the read cell content to reference voltage levels to determine the data stored in the corresponding memory cell. Likewise, similar functions are performed by the redundant y-driver circuit for the redundant memory array. During the verification of the contents of the memory cell, if the read voltage is outside a certain margin requirement for a level of the reference voltage, a signal is generated in real time so that data from the bad y-driver is not output and data from the redundant y-driver corresponding to the redundant memory array is read out. The memory array system may also include a fractional multilevel redundancy.